ATTACHMENT: VERSION WITH MARKINGS SHOWING CHANGES MADE

IN THE SPECIFICATION:

Page 6, line 4, please add the following new paragraphs:

--Fig. 10 is a pictorial representation (through a cross-sectional view) showing a field effect transistor (FET) of the present invention.

Fig. 11 is a pictorial representation (through a cross-sectional view) showing a capacitor structure of the present invention.--

Page 11, line 27, please add the following new paragraphs:

Fig. 10 illustrates a cross-sectional view of a FET which includes the metal silicate described above as a dielectric material. Specifically, the FET shown in Fig. 10 includes Si-containing semiconductor substrate 11 having spaced apart source and drain regions 20 and 22, respectively defining channel 24 located therein. The FET also includes SiO_2 layer 16 located above channel 24, metal silicite layer 14 located atop SiO_2 layer 16, and gate electrode 26 located atop metal silicate layer 14. The gate electrode comprises polysilicon, W, Al or Pt.

Fig. 11 illustrates a cross-sectional view of a capacitor which include the metal silicate described above as a dielectric material. Specifically, the capacitor structure includes conductive electrodes 30 and 32 respectively, and SiO_2 layer 16 and metal silicate layer 14 sandwiched therebetween.--

IN THE CLAIMS:

Please cancel Claim 32 as well as non-elected Claims 1-20 and please amend Claims 21, 28 and 34 as follows:

✓ 21. (Twice Amended) A semiconductor structure comprising at least one metal silicate dielectric material that is [formed on] in direct contact with a silicon oxide layer, said silicon oxide layer being formed on a Si-containing substrate.

~~29~~. (Amended) A field effect transistor comprising:

a Si-containing semiconductor substrate;

spaced apart source/drain regions in said substrate defining a channel region therein;

a dielectric layer located atop [above] said channel region, said dielectric layer including a [first] bottom SiO_2 layer [of a] and a top metal silicate layer; and

a gate electrode formed over said [dielectric] top metal silicate layer.

✓ 34. (Thrice Amended) A capacitor comprising [at least one] a metal silicate dielectric material and a SiO_2 layer sandwiched between [the same or different] top and bottom electrode materials, wherein said at least one metal silicate is located directly atop said SiO_2 layer [obtained by forming a metal oxide layer on a silicon-containing material and heating said metal oxide layer in the presence of an oxidizing agent under conditions so as to convert said metal oxide layer into said metal silicate while simultaneously oxidizing a portion of the silicon-containing material underlying the metal silicate].